

# OneSpin 360 EC – FPGA

## THE SEQUENTIAL EQUIVALENCE CHECKING SOLUTION FOR ADVANCED SYNTHESIS-OPTIMIZED FPGAs

### HIGHLIGHTS

- Ensures that highly optimized, complex FPGA designs are free of synthesis and optimization errors
- First equivalence checker to support *all* sequential synthesis optimizations in large FPGA devices
- Enables competitive FPGA functionality, performance, power, and cost
- Verifies the FPGA design “as is” without simulation, design modifications or restrictions

### OVERVIEW

The OneSpin 360™ Equivalence Checker for field-programmable gate array designs – 360 EC-FPGA for short – detects functional errors and mismatches that can be introduced by advanced FPGA synthesis optimizations, that are commonly used to achieve the competitive functionality, performance, power consumption, and cost targets, of FPGA designs. It is the *first* tailor-made FPGA equivalence checker to support *all* sequential synthesis optimizations performed in large FPGA devices.

The 360 EC-FPGA solution addresses the challenge of comparing two design representations in which sequential optimizations generate non-corresponding state structures. FPGA-specific optimizations typically invalidate the working hypothesis of state correspondence used by most ASIC equivalence checkers, making it impossible for them to perform FPGA design verification without disabling optimizations and simultaneously incurring extensive manual effort to apply them to FPGA flows. 360 EC-FPGA thus eliminates the significant productivity barriers that restrict the use of conventional ASIC equivalence checkers in FPGA verification.

The 360 EC-FPGA solution efficiently verifies the optimized design “as is” without time-consuming simulation and without the design modifications and restrictions imposed by other

equivalence checkers. 360 EC-FPGA verifies whole-chip flat netlists, which enable the most aggressive optimizations. Consequently, the designer can develop a highly competitive design, uncompromised by verification constraints.

The new 360 EC-FPGA is an innovative, sequential FPGA equivalence checker that thoroughly proves, that design functionality is maintained through all implementation phases of an FPGA design. It is an automatic, synthesis-tool-independent solution that verifies functional equivalence between the register transfer level (RTL) code and the post-synthesis netlist, as well as between the post-synthesis netlist and the post-place-and-route netlist. Moreover, it does not rely on information in “side files” generated by synthesis tools and extensive scripting – both typically required by ASIC equivalence checkers when used in FPGA design verification.

The solution seamlessly works with the established Synopsys® Synplify Pro/Premier® synthesis flows, Altera’s Quartus II® as well as Xilinx ISE® flows and supports all major FPGA product families from Actel, Altera and Xilinx, for both post-synthesis netlists and post-place-and-route netlists.

The 360 EC-FPGA solution simplifies and accelerates otherwise time-consuming – or even impossible! – verification and debug tasks through:

- Automation of design consistency checking, design initialization, state mapping, sequential compare, and sign-off
- A fully-featured debug environment that locates the root cause of synthesis and optimization errors
- A flow-based graphical user interface and Tcl shell
- Seamless integration into existing verification flows

Consequently, the 360 EC-FPGA solution meets the high-quality verification and time-to-market objectives critical to the two main FPGA use models:

- Prototyping to validate complex functionality enabling rapid ASIC design and early software development
- Production, where the FPGA is the final implementation platform

## VERIFICATION FLOW

The 360 EC-FPGA verification flow proceeds in four steps: design consistency checking, automatic state initialization and port mapping, automatic state mapping, and sequential comparison and debug (see Figure 1).

### Design Consistency Checking

In addition to extensive sequential design checks, 360 EC-FPGA automatically generates a comprehensive set of RTL checks to identify, for example (from a long list) dead code, simulation/synthesis mismatches, race conditions, bus contention, X-assignments, and user-defined assertions in the early design phases. The generated assertions are then exhaustively proven.

### Automatic State Initialization and Port Mapping

360 EC-FPGA automatically computes an initialization sequence of primary input stimuli and

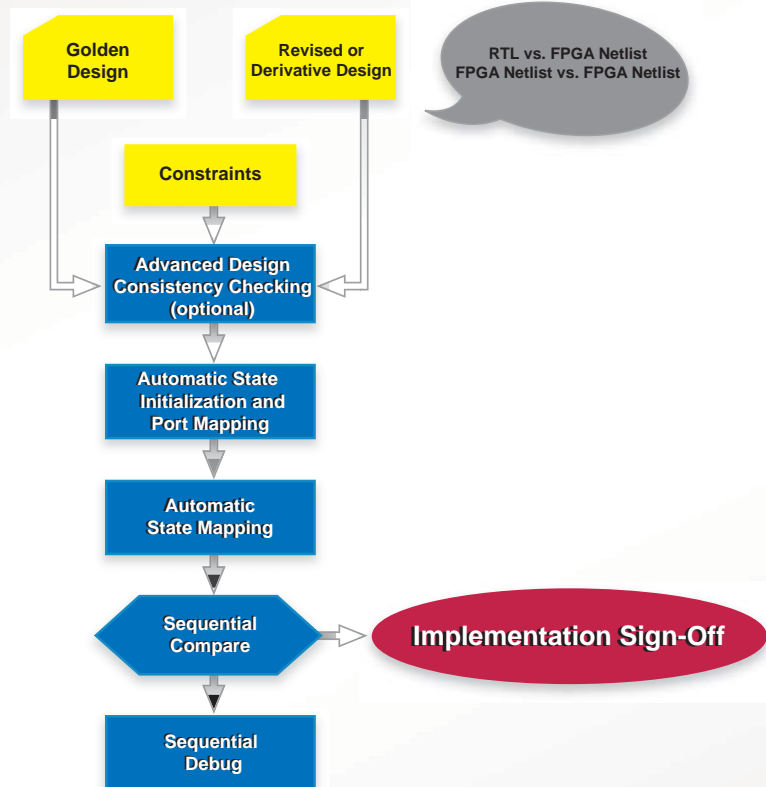


FIGURE 1: THE ONESPIN 360™ EC-FPGA VERIFICATION FLOW

resets the two design representations that are to be compared to a known initial state. This is essential to subsequent sequential comparisons, which prove that the compared design representations exhibit identical behavior from their respective initial states onwards.

### Automatic State Mapping

Automatic, functional state mapping is applied to handle the most frequent FPGA optimizations, such as state (flip-flop/latch) duplications and merges, as well as constant state propagations. State mapping inserts additional mapping points to handle aggressive synthesis optimizations such as retiming or pipelining.

### Sequential Comparison and Debug

If the automatic, sequential compare succeeds, the two design representations are confirmed to be functionally equivalent – sign-off for this implementation step is achieved. If the comparison fails, the 360 EC-FPGA sequential debugging environment generates an undisputable, reachable counterexample, and displays it as a waveform. The solution’s debug capability facilitates a systematic and well-structured debug approach to accelerate the localization of the root cause of functional differences. This includes value annotation of source code, schematic engine, hierarchy browser, as well as driver and load tracing (see Figure 2).

## KEY FEATURES

### Verification Features

- Supports all sequential optimizations in FPGA synthesis, including:
  - Stuck-at (constant) registers
  - Register duplication and merging, independent of net/instance name modifications
  - Gated clock conversions
  - Retiming and pipelining support
- Computes initialization sequences and verifies the design’s initial state
- Supports DSP optimizations
- Imposes no restrictions on netlist size
- Verifies flat netlists – no need to preserve hierarchy
- Deploys a high degree of automation and simple scripting to accomplish complex tasks
- Does not rely on synthesis side files such as “Verification Interchange Format” (.vif)
- Integrates with the design team’s existing FPGA design flow “as is”
- Focuses debug with logic cone extraction and highlighting

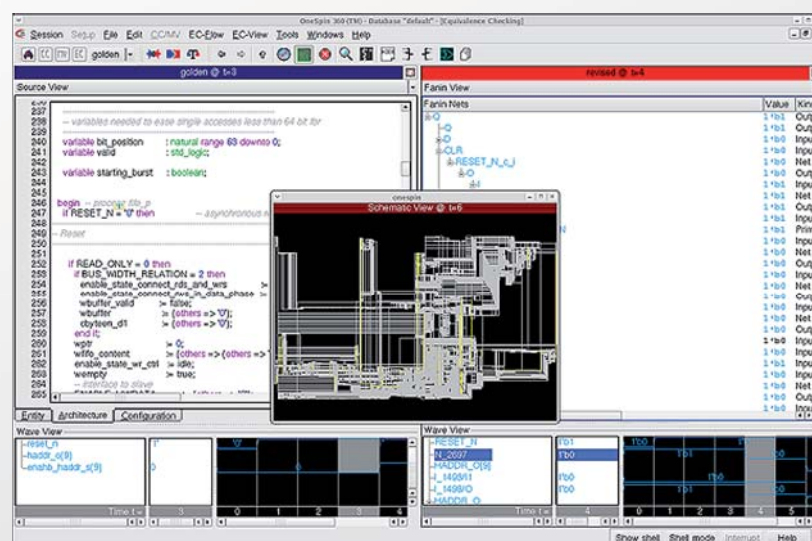


FIGURE 2: THE 360 EC-FPGA DEBUG ENVIRONMENT



- Detects synthesis bugs, synthesis/simulation mismatches and RTL coding bugs that might otherwise be overlooked by less advanced equivalence checkers, including:
  - Synthesis full\_case and parallel\_case
  - Bus contention and floating
  - Division by zero
  - Negative divisor, exponent or remainder
  - Don't care and X assignment
  - Read/write, write/write race conditions
  - Function without return
  - Array boundary violations
  - Range overflow
  - Stuck-at
  - Initialization errors
  - Dead code

#### **Design Flow Support**

OneSpin 360™ EC-FPGA supports major synthesis flows including Synopsys SynplifyPro/Premier®, Altera's Quartus II® and Xilinx ISE®.

#### **FPGA Product Family Support**

All major device families from Actel, Altera and Xilinx are being supported.

This support as well as the design flow support is subject to ongoing expansion, so please contact OneSpin Solutions for the latest status.

#### **Platform Support**

360 EC-FPGA supports popular computer platforms, including Linux 32/64 bit (Opteron/Xeon) and Solaris 32/64 bit.

#### **Packaging**

The 360 EC-FPGA solution is available as a single vendor license for either Actel, Altera or Xilinx devices or as a full license that includes all device families.

## **FPGA PROTOTYPING AND PRODUCTION**

360 EC-FPGA leverages more than a decade of technology and methodology development of 360 EC-ASIC, OneSpin's established equivalence checking solution for ASIC flows. For more information on the ASIC equivalence checking solution, please refer to the 360 EC-ASIC data sheet.

## **CONTACT ONE SPIN SOLUTIONS**

FOR FURTHER INFORMATION PLEASE VISIT [HTTP://WWW.ONESPIN-SOLUTIONS.COM](http://www.onespin-solutions.com)  
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