

OneSpin Solutions Customer Success

INFINEON PROTOCOL PROCESSOR

➤ USED 360 MV TO ACHIEVE ERROR-FREE FUNCTIONAL OPERATION AND SLASH VERIFICATION EFFORT BY 40%

CUSTOMER PROFILE

The Intellectual Property & Reuse department (IPR) of Infineon's Communication Solutions business group (COM) supplies COM's worldwide product groups with in-house and third party intellectual property (IP) components. In order to meet time to market and profitability objectives, IPR deploys a comprehensive IP reuse strategy. IPR must ensure both right-first-time functional behavior and early availability of the IP. Consequently, IPR's mandatory verification procedures employ advanced testbench automation and formal verification techniques.

BUSINESS CHALLENGE

The IPR department developed a network processor – the PPv2 – to meet the demanding throughput requirements of COM's wire-line chips across a wide range of applications from digital subscriber line (DSL) to routers. IPR had to optimally meet three conflicting challenges:

- Ensure cost-effective risk-free reuse across a wide variety of applications.
- Provide the highest quality essential to error-free functional operation of both hardware and software.
- Constrain the R&D effort to that of PPv2's predecessor, which had not been designed for wide reuse.

VERIFICATION OBJECTIVES

The PPv2 is a compact, high-performance, configurable 32-bit RISC processor with an application specific set of 40 instructions, a seven-stage pipeline and fine-grained multi-threading. Its development leveraged the design of an earlier protocol processor, PPv1, but required far-reaching changes that made it essentially a "from scratch" design. Some of the verification challenges included:

- Ensure the correct pipelined processing of multiple instructions, guaranteeing no undesired interferences between instructions; and ensure the correct operation of permissible – but unpredictable – behaviors such as traps and interrupts.
- Guarantee transparency of pipelining together with related forwarding and stalling behavior to the software programmer.

- Comprehensively verify data paths with complex bit-manipulations.
- Meet hard real-time requirements such as trap- and interrupt-execution within permissible latencies.
- Ensure independent execution of multiple threads under all possible combinations of instructions, thread switches and permissible, but unpredictable, behaviours.
- Precisely describe the integration requirements of any hardware/software environment into which the PPv2 would have to be integrated.

VERIFICATION STRATEGY

The behaviours to be verified are high level processor transactions. IPR considered it impossible to use register transfer level (RTL) simulation and RTL-based formal verification tools to (a) describe PPv2's hardware/software operating environments and (b) verify the complex transactions of (for instance) an intricate pipeline operation, with all of its configuration and context switching combinations. Moreover, IPR concluded that RTL verification approaches were not practical even as a backup strategy. IPR thus required a formal verification solution that operates at the transaction level – and one that it could trust.

Infineon had already used OneSpin's technology to successfully verify a far larger, superscalar 32-bit processor for automotive applications, proving it to be fully compliant with its programmer's model. Consequently, IPR selected OneSpin's 360 Module Verifier (360 MV for short) to verify PPv2.

„USING ONESPIN TECHNOLOGY, WE FULLY VERIFIED THE PPV2 PROTOCOL PROCESSOR INCLUDING ITS ADVANCED CONTEXT SWITCHING, WHICH IS A CENTRAL IP COMPONENT OF OUR COMMUNICATION APPLICATIONS. THIS VERIFICATION APPROACH ASSURED THAT THE COMPLETE FUNCTIONALITY OF THE PPV2 WAS COVERED AND BUG ESCAPE ROUTES BLOCKED. MOREOVER, THE TOTAL VERIFICATION EFFORT WAS ABOUT 40% LESS THAN THAT IN A PREVIOUS, SIMULATION-BASED PROJECT“.

Alexander Haggemiller, Director of the Intellectual Property & Reuse Department of Infineon Technologies

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VERIFICATION APPROACH

The PPv2 specification defines how instructions modify registers that are visible to the programmer, for instance program address, register file, and status flags; describes memory traffic for instructions and data; and defines the desired response to permissible, but unpredictable, behavior.

For each instruction, the team developed a property that describes how the instruction passes down the pipeline and how it influences the implementation signals and registers. The team then developed a high-level view of that property that co-relates the implementation registers with the specification registers to check compliance between the two. This is a non-trivial achievement because results computed by an instruction must typically propagate through the pipeline before they are stored, and are subject to unpredictable forwarding or stalling.

The team then used 360 MV's property checker to debug the property and its associated VHDL code. Within seconds, the checker computed a waveform diagnostic counter-sequence. The team then used the 360 MV's debugger to navigate through the property hierarchy, automatically highlighting the abstract variables and signals likely to explain the counter-example.

An example of a complex behavior to be analyzed is that of a branch instruction, for which a static parameter configures execution of up to four delay slots. Upon receiving an interrupt, these slots must be stored, then executed after the interrupt. This sequence must behave correctly in a wide range of configurations. Using 360 MV, the team detected a configuration in which the slots were only partially executed. The VHDL description was corrected, and specification ambiguities and flaws were removed.

Another example is that of a property gap. Using 360 MV, the team found that instruction words had been modified while stored in the context switch buffers. This rare phenomenon had not been considered in the specification – and would most certainly have escaped any simulation-based verification.

When all properties were proven, specification compliance had been shown for the behavior that the properties captured. The team then used 360 MV's automatic completeness analysis to confirm that every possible behavior of the PPv2 had been captured by these properties.

RESULTS

IPR achieved True Functional Sign-Off for PPv2, using OneSpin's 360 Module Verifier. The project met all of its stated objectives.

The 360 MV formal verification and debug methodology:

- Achieved error-free functional operation of the entire PPv2 across all possible configurations.
- Implied correct PPv2 operation in hardware/software environments that meet three well-defined integration requirements.
- Achieved all of this with 4 engineer-months of effort. The total verification effort was 40% less than that of PPv1.

A few details: verification was based upon a written specification of 130 pages, containing a number of ambiguities and unspecified situations, and 11,000 lines of unsimulated, newly developed VHDL. Using 360 MV, the team:

- Acquired a thorough understanding of the PPv2 architecture; and generated well-specified integration requirements.
- Found 10 serious errors and 17 other issues that required specification modification and redesign of the context switch logic
- Ensured that the VHDL correctly implemented the specification, and that no functionality had been overlooked.
- Generated a suite of 38 proven properties, unambiguously describing the PPv2's cycle-accurate behavior, on fewer than 40 easily read pages.
- Produced – purely as a by-product – a formal, executable programmer's view in the form of a transaction level model (TLM) of just 10 pages, which was provably sequentially equivalent to the VHDL.

Moreover, the verification infrastructure comprised only one standard workstation and one 360 MV license. The entire property suite ran easily overnight on this workstation, enabling immediate verification of code changes.

CONCLUSIONS

OneSpin's technology ensured error-free functional operation of the Protocol Processor PPv2, accurately predicted its behavior in the target hardware/software environments; detected errors and omissions in the specification; and therefore enabled True Functional Sign-Off. The technology also slashed verification efforts by 40%, and reduced chip-level functional verification effort by providing precisely defined integration requirements.

For IP such as the PPv2, 360 MV perfectly fulfilled the needs of both IP providers and IP integrators.